Practical Spread-Spectrum: Clock Recovery With the Synchronous Oscillator

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Introduction

Clock recovery circuits are usually built around convolvers, such as surface acoustic wave devices, or phase-lock loops such as Costas loops, τ-dither loops etc (see references 1, 2). The formers tend to be extremely expensive and therefore out of the reach of radio amateurs, while the latters can be quite complicated and are inclined to work better when the clock information is present most of the time.

When, however, synchronization information is missing, a large portion of the time (ie, in the presence of heavy interference, or long pseudorandom sequences) most PLLs revert quickly to their free-running frequency, thus producing output jitter.

A simple solution to the above problem is the Synchronous Oscillator (SO), an interesting and simple circuit which can be used for clock recovery. This article describes its principle, as well as a test apparatus designed to evaluate the SO's practicality, ease of use, and performance.

The Basic Circuit

Referring to Fig 1, the Synchronous Oscillator is basically a modified Colpitts oscillator with an extra transistor in its emitter-to-ground path. It has two positive feedback paths: one from the junction of the two capacitors in the collector tank circuit back to the emitter of the upper transistor; the other one from the junction between the tank coil and the RF choke back to the base of the transistor. The operation of this circuit is described in detail in references 3, 4 and 5. Briefly, the upper transistor is a free-running sinusoidal oscillator operating in class C. It thus conducts only during very short periods of time. Whenever it draws current, it develops a voltage across the bottom transistor, and allows the latter to conduct. Therefore, of all the signals applied to the base of the bottom transistor, only those which appear during that very short "time-window" which is the moment of conduction, can be amplified by the bottom transistor and used to synchronize the upper one. This "coherent amplification" arrangement

explains the excellent noise rejection characteristics of the SO. (Such a circuit is used for carrier recovery in my 440 MHz direct-sequence spread-spectrum link, published in the May 1989 issue of QST.) Note that, contrarily to what happens in a phase-lock loop, in an SO the input signal directly synchronizes the output signal.

The Clock Recovery Circuit

Clock recovery circuits do not generally need the ability to work with noisy signals, a quality usually demanded of carrier-recovery circuits, and it is thus possible to further simplify the SO (see Fig 2). The tuned circuit in the collector introduces a flywheel effect which supplies the stability required to produce steady output clock pulses in the momentary absence of input synchronization pulses.

Practical Application

To put the SO to the test, an apparatus was built which generates an incomplete train of synchronization pulses. (In other words, properly timed synchronization pulses are produced, but some of them are purposely deleted.) The general arrangement is shown in Fig 3, while the actual circuit is shown in Fig 4.

U1, a crystal oscillator operating at 2 MHz is used to drive a seven-stage pseudorandom noise (PN) generator of the kind used in most of my spread-spectrum equipment. The PN generator consists of U2, a 74164 shift register, while two sections of U3, a 7486, are used as an XOR and inverter stage (see reference 6 for a more complete description of the PN generator used). This PN sequence is fed to an "edge-detector" consisting of U4, another 7486 XOR integrated circuit. Three of the four gates are connected in series, and their cumulative propagation delay is put to good use to retard the incoming pulse. This pulse and the original pulse are XORed in the fourth section of U4, and a short output pulse is thus created for each input transition. Since the output of a seven-stage pseudonoise generator presents at times up to six "0" or six "1"
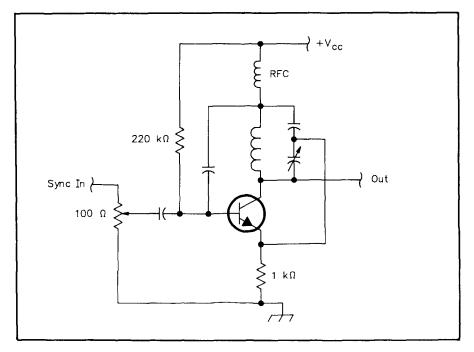

Fig 1—The Synchronous Oscillator. Component values depend on frequency of interest and transistors used.
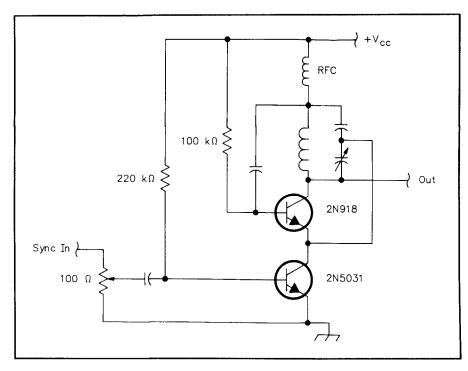
Fig 2—Simplified Synchronous Oscillator for clock recovery.

in a row, the edge-detector will create a pulse train with up to six synchronization pulses missing from time to time.

This latter pulse-train is the synchronization information supplied to our SO. It is displayed on the lower oscilloscope trace of Fig 5. One of the characteristics of the SO, which consists of Q1, is that it is a sine-wave oscillator whose output amplitude is always constant throughout the synchronization range. Since the output amplitude is constant, it is acceptable to feed it to a CMOS Schmitt trigger (U5, a 74HC14) without fear of output jitter. (Which would otherwise result from variable trigger points due to the ceaselessly varying slope of a variable amplitude signal, should such a signal be used.) The

output of the Schmitt trigger stage is a 2-MHz square wave shown on the upper oscilloscope trace of Fig 5. Notice that, although 6 synchronization pulses are missing, there is no visible jitter on the traces in the interval between sync pulses.

Construction

The circuit described above was constructed on perforated phenolic board, using point-to-point wiring techniques and generally following good HF wiring practices, particularly with regard to grounding and decoupling. If it is desired to recover clock frequencies much above 50 MHz, the circuit can be scaled up, but it will be necessary to use

Schmitt triggers made of discrete components (such as MPF102 FETs). Similarly, VHF transistors (such as the 2N918) should replace the 2N2222 used for Q1.
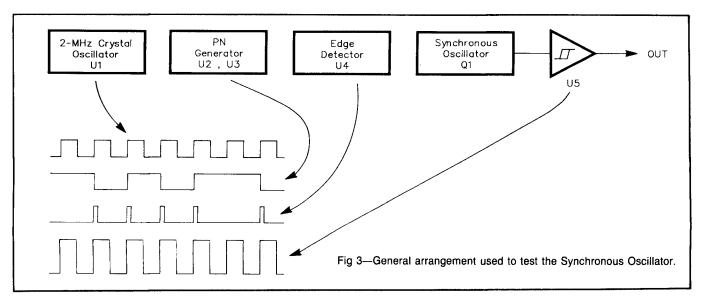
Adjustments

A digital frequency counter is connected to the output of U4 (pin 11). The wiper of R1, the potentiometer used to adjust the amount of sync signal applied to the SO, is first turned all the way down to ground. The slug of L2 is then adjusted to bring the free-running frequency of the SO near the target frequency (in our case, 2 MHz). The variable capacitor C1 is then adjusted until the output frequency, read on the frequency meter, is as close as possible to the target frequency (say plus or minus 5 kHz, or between 1,995 and 2,005 MHz). The input signal is then slowly increased by means of R1. After less than ¼ turn, the frequecy meter will suddenly display the target frequency, as the SO has reached lock.
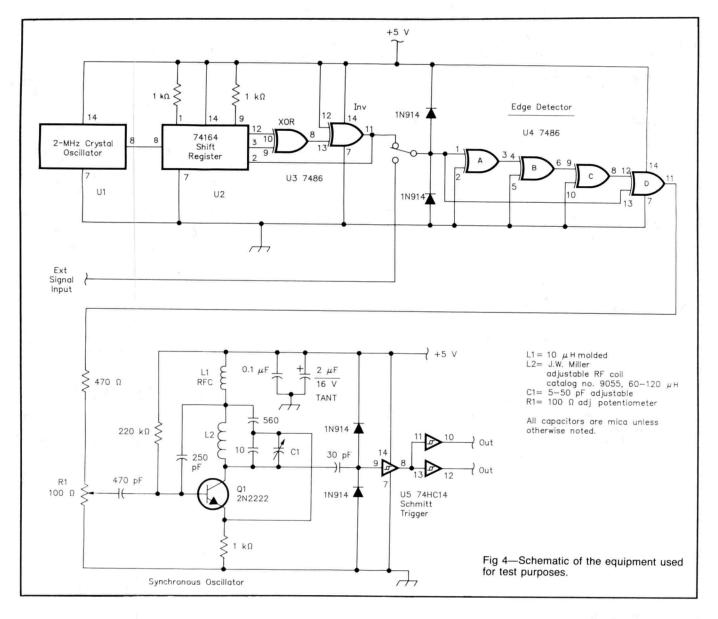
If a dual-trace oscilloscope is available, connect channel B to the output of the edge-detector U4, connect channel A to the output of U5 and synchronize on channel A. The channel (the upper trace on Fig 5) will display a square wave, while the other trace will be fuzzy. As you slowly turn up R1, the lower trace (channel B) will suddenly synchronize with the bottom trace, as shown on Fig 5.

Tracing Range

To simulate the effects of a Doppler shift in input frequency (satellite operation, for instance), the crystal oscillator was replaced by a variable-frequency oscillator. Which the values shown on Fig 4 and the circuit adjusted for a free-running frequency of 2 MHz, the tracking range (ie, the bandwidth within which synchronization takes place without returning) extended from 1.986 MHz to 2.015 MHz. This 1.5 tracking range is generally in agreement with measurements reported in references 3 and 4. Several

Fig 3—General arrangement used to test the Synchronous Oscillator.

Fig 4—Schematic of the equipment used for test purposes.

Within the schematic:

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+5 V

2-MHz Crystal Oscillator  U1
74164 Shift Register  U2
1 kΩ   1 kΩ
XOR  U3 7486
Inv
1N914
1N914
Edge Detector  U4 7486
A  B  C  D

Ext Signal Input
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L1 = 10 μH molded
L2 = J.W. Miller
     adjustable RF coil
     catalog no. 9055, 60–120 μH
C1 = 5–50 pF adjustable
R1 = 100 Ω adj potentiometer

All capacitors are mica unless
otherwise noted.
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Synchronous Oscillator components: 470 Ω, 220 kΩ, 470 pF, R1 100 Ω, L1 RFC, L2, 250 pF, 560, 10, C1, 0.1 μF, 2 μF 16 V TANT, +5 V, 1N914, 30 pF, 1N914, Q1 2N2222, 1 kΩ, U5 74HC14 Schmitt Trigger, Out, Out

typical synchronization curves have been published in reference 3. It should be kept in mind that the tracking range depends on the level of the synchronization signal at the input, and on the Q of the collector tank circuit. (Incidentally, per reference 7, the maximum doppler shift created by amateur radio satellites is typically less than 0.006 which is but a fraction of the tracking range available with the SO.)

Conclusion

The SO is a circuit remarkable both for its performance and its simplicity of construction. The reader is encouraged to breadboard a SO to appreciate its ease of use. (If a commercial application is contemplated, the reader should note that the SO is covered by several US patents, see note 8.)

I am indebted to Professor Marvin White (of Lehigh University) and Mr. Vasil Uzunoglu (formerly with Fairchild Communications), the co-developers of the Synchronous Oscillator, for their encouragements and stimulating discussions.

References

[1] R. Dixon, *Spread Spectrum Systems*, (New York: Wiley) 2nd Ed, 1984, pp 186-187 and pp 232-234.
[2] R. Best, *Phase-Locked Loops*, (New York: McGraw Hill) 1984, pp 212-217.
[3] V. Uzunoglu and M. White, "The Synchronous Oscillator: A Synchronization and Tracking Network," *IEEE Journal of Solid State Circuits*, Vol SC-30, No. 6, Dec 1985, pp. 1214-1224.
[4] V. Uzunoglu and M. White, "Some Important Properties of Synchronous Oscillators," *Proceedings of the IEEE*, Vol 74, No. 3, Mar 1966, pp 516-518.
[5] A. Kesteloot, "Extracting Stable Clock Signals from AM Broadcast Carriers for Amateur Spread-Spectrum Applications," *QEX*, October 1987, pp 5-9.
[6] A. Kesteloot, "Practical Spread-Spectrum: A Simple Clock Synchronization Scheme," *QEX*, October 1986, pp 4-7.
[7] M. Davidoff, *The Satellite Experimenter's Handbook*, (Newington, CT: ARRL), 1984, pp 10-3 to 10-5.
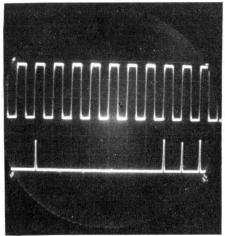[8] US Patents 4,274,067; 4,355,404; 4,356,456.

Fig 5—The upper oscilloscope trace shows the output of the Synchronous Oscillator (U5, pin 8) while the lower trace shows the train of synchronization pulses. Note that there is no visible jitter on the output signal in the absence of input signal. Horizontal scale: 0.5 μSec/division.